REMARKS

Claims 1-14 are presented for examination. Claims 12 and 14 are found allowable subject to being rewritten in independent form. Claims 11-14 have been cancelled.

Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudo et al. on view of Geldman et al.

This rejection is respectfully traversed for the following reasons.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As demonstrated below, the combined teachings of Kudo et al. and Geldman et al. are not sufficient to arrive at the invention recited in claim 1.

In particular, claim 1 recites a microprocessor including:

- a program control unit controlling fetch of an instruction code;

- an instruction decode unit decoding said fetched instruction code;

- an address operation unit operating an address of a memory on the basis of the result of decoding by said instruction decode unit; and

- a data operation unit operating data on the basis of the result of decoding by said instruction decode unit.

The claim specifies that the data operation unit executes data transfer between registers and data transfer between said registers and said memory in correspondence to single said instruction code having a single operation code fetched by said program control unit.

In the previous Response, Applicant submitted that the claim recites execution of data transfer between registers and data transfer between the registers and the memory in correspondence to a single instruction code having a single operation code, whereas Geldman discloses instruction MV8 for copying the contents of register b into register a (col. 8, lined 16-19).

In the present Office Action, the Examiner indicates that Geldman was relied upon only for teaching of data transfer between registers in accordance with a single instruction MV8.

Accordingly, the Examiner admits that Geldman does not disclose data transfer between registers and data transfer between the registers and the memory in correspondence to a single instruction code having a single operation code, as the claim requires.

Further, the Examiner asserts that the data transfer between registers and memory is taught by Kudo. Accordingly, the Examiner realizes that Kudo does not disclose the data

transfer between registers and data transfer between the registers and the memory in correspondence to a single instruction code having a single operation code, as the claim requires.

Hence, the Examiner realizes that neither Kudo nor Geldman suggests both data transfer between registers and data transfer between the registers and the memory in correspondence to a single instruction code having a single operation code.

It is respectfully submitted that since none of the references suggests both data transfer between registers and data transfer between the registers and the memory in correspondence to a single instruction code having a single operation code, a combination of Kudo with Geldman would not suggest this feature.

Instead, the combined teachings of the Kudo and Geldman references would suggest a data transfer between registers in accordance with one instruction, and a data transfer between the registers and the memory in accordance with another instructions.

Further, it is noted that instruction MV8 of Geldman for data transfer between registers (col. 8, lines 7-19) is composed of multiple operation codes rather than of a single operation code, as the claim requires.

Accordingly, the composed teachings of the applied references would not be sufficient to one of ordinary skill in the art to suggest the data transfer between registers and data transfer between the registers and the memory in correspondence to a single instruction code having a single operation code, as claim 1 requires.

Hence, the Examiner's conclusion of obviousness with respect to claim 1 is not warranted.

Dependent claims 2-8 are defined over the prior art at least for the reasons provided above in connection with claim 1.

Therefore, Applicant respectfully submit that the rejection of claims 1-10 under 35 U.S.C. 103 is improper and should be withdrawn.

In view of the foregoing, and in summary, claims 1-10 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

Entry of the amendment of claims under 37 CFR § 1.116 is respectfully requested because the amendment is limited to cancellation of claims 11-14. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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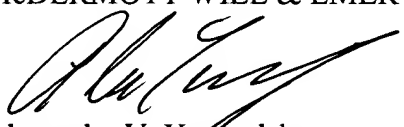

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